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Optimization of Power System Transients in a Multi-Machine System using Unified Power Flow Controller

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Abstract:

For better utilization, the current system is now equipped with Flexible AC Transmission System (FACTS) devices. The Unified Power Flow Controller (UPFC), a multi-machine system coupled FACTS device, is discussed in this work along with its modelling and simulation. The effectiveness of these controllers is evaluated and the results of the minimization of the settling time of power oscillations and transient peaks of line power, bus voltages, and rotor angle between two machines, respectively, for single line to ground and three-phase fault. A thorough analysis shows that a three-phase failure is more serious than a single line to ground fault. The findings also suggest that the proposed controller improved the stability of a particular system by reducing oscillations in the power system and stabilizing the test system. In this article, a PI controller approach for UPFC is used to control power flow and voltage at matching buses. The control strategy is evaluated for the IEEE-9 bus power system network using Matlab/Simulink.

Keywords: FACTS, SSSC, STATCOM, UPFC, Pi Controller.

I. Introduction

The present power system consisting of a complex power system network with the number of generating units interconnected. The power system's efficiency is decreased by this complexity, which also adds instability. The electrical power sent along a line is determined by the voltages at the receiving and transmitting ends, the angle of phase between them, and the line impedance. The maximum power carrying capacity and power flow of existing transmission lines can both be increased using FACTS [1,3] devices. The FACTS controller can generally be divided into three categories: mechanical switches, voltage source converters (VSC), and hybrid devices. In Fig. 1, various VSC FACTS devices are shown, including the two-port Unified Power Flow Controller (UPFC) [2,3] and Interline Power Flow Controller (IPFC) [3][12] and the one-port Static Synchronous Compensator (STATCOM) and Static Synchronous Series Compensator (SSSC) [3].

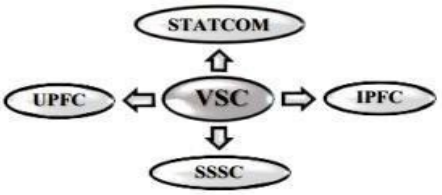


Fig.1: Different FACTS devices based on VSC

One of the most flexible and effective FACTS devices, UPFC may improve the stability of the power system and provide superior power flow. On using UPFC in power systems, there are numerous articles and technical publications. In order to control the natural power-sharing between the two distinct parallel transmission lines and enable the maximum transmission capacity for efficient utilisation, the Thyristor Controlled Series Compensator (TCSC) [3][13] and UPFC are installed in the power system. The UPFC is a FACTS controller of the series-shunt mixed type. It is employed to control bus voltage, reactive power, and real power. The phasor model of UPFC [8][14] is utilised in this study to evaluate the usage of UPFC in power flow control in the IEEE-9 [4] bus power system. The simulations are performed using the Matlab/Simulink software package.

II. Test System Description

Figure 2 displays a single line representation of a 9-bus system. The system is designed as a loop, with three transformer banks (16.5/230kv, 13.8/230kv, and 18/230kv) and nine buses (B1 to B9) connected by transmission lines with periods ranging from one to three phases. and Three loads are connected to bus as show in fig 2(100MW,125MW,90MW) and three generators are used namely power unit-1 is consider as swing generator, Power unit -2 & Power unit-3 are consider as pv generator(246MW,125MW, 180MW) . The test system model, shown in Figure 3, has an IEEE 9 bus, three machine systems, 50 km, and 230 kV.

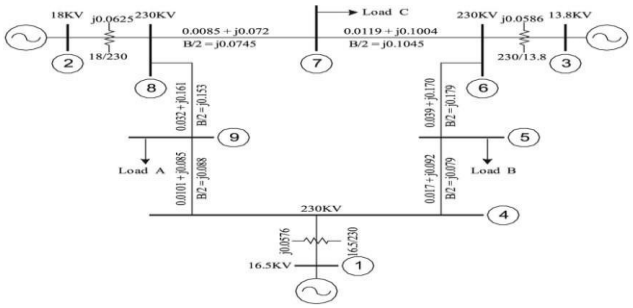


Fig 2: Single line diagram of IEEE nine bus system

III. SIMULATION LINK MODEL OF UPFC

A nine-bus system was used to test the adoption of UPFC to increase voltage stability. The investigation begins with a nine-bus system with and without UPFC [10][11][15]. The IEEE9 bus system is then simulated using MATLAB software. To enhance the voltage profile, a UPFC was applied to each of the nine bus systems' output results. UPFC is connected to a transmission line in between bus no.8 & bus no.9 as show in fig 3.1.

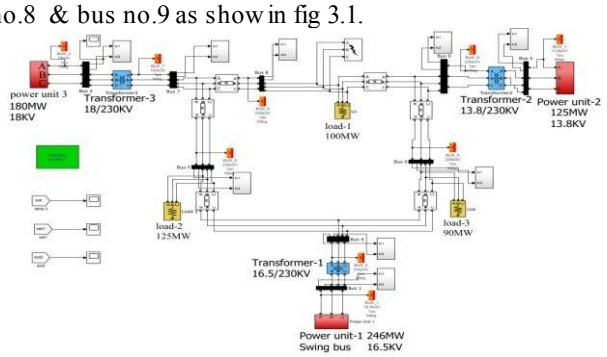


Fig 3: Nine bus system simulation diagram without UPFC

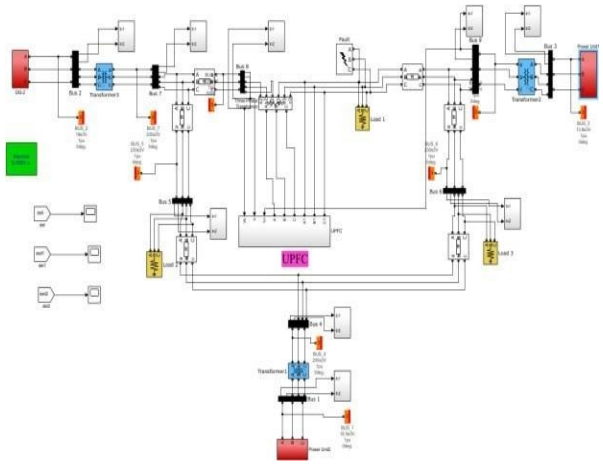


Fig 4: Nine bus system simulation diagram with UPFC

The system has been looked into first for the uncompensated system and subsequently for the system using UPFC. After comparison, it was discovered that adding UPFC to the system improves system performance. This paper validates and assesses the performance of the proposed controller using three different fault types.

IV. UPFC INSIDE BLOCK DIAGRAM

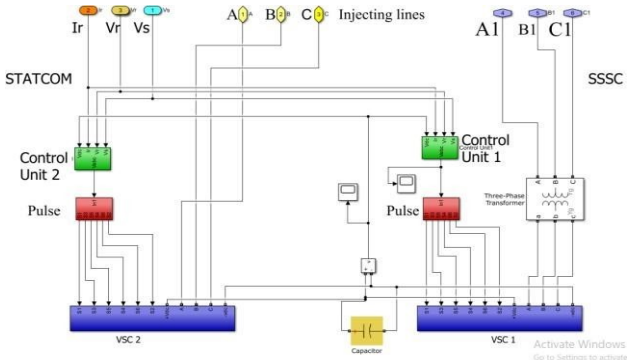


Fig 5: Simulink UPFC inside block.

A. PI CONTROL BLOCK

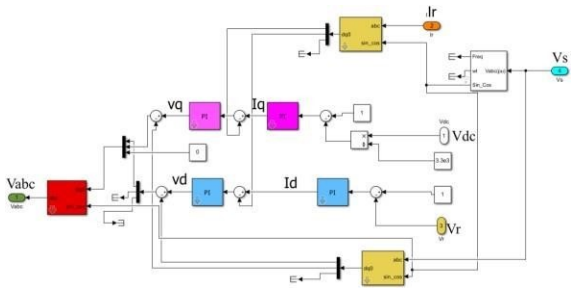


Fig 6: Simulink PI controller

PI Controller consist of two loop namely AC voltage control loop & DC voltage control loop as shown in fig 6.

i. AC VOLTAGE CONTROL LOOP ORDIRECT TRANSFORMATION

The AC voltage values come from receiving voltage Vr[0.7V], receiving voltage value is measured with per unit value [1].both Vr &PU values are different, then its error signal is given to pi controller, PI controller generates direct current Id[1A], this Id current is measured with receiving current[-1.17A], this error signal is given to PI controller blocks, PI controller block generates direct voltage Vd[1v], direct voltage is measured with sending voltage Vs[0.81V] then error signal is given to the compensation voltage block.

ii. DC VOLTAGE CONTROL LOOP OR QUADRATURE TRANSFORMATION

DC voltage values from capacitor Vdc [2.4kv] This value is compared with constant voltage [3.3KV], this error signal value is compared with per unit value [1PU] again error signal value is Given to the PI controller block, PI controller block generate the the Iq current this Iq current [1A] is measured with receiving current [3.67A] then again error signal is given to PI controller block, PI controller blocks generate Vq voltage this Vq voltage is measured[Vq=0] with source voltage Vs [-0.05125v]This error signal is given to compensation voltage block.

iii. ZERO TRANSFORMATION

Constant zero signals error value is given to the compensation voltage block Finally we get three signals, these signals DQ0 reference frame is converted to Vabc reference with the help of Park transformation. Vabc value is given to the pulses converter.

B. PULSES

Three phase voltage is from PI controller Vabc. According to the system voltage AC voltage control and DC voltage control we can inject real and reactive power using inverter device for that only pulses needed.
Here, two signals 1. Carrier signal, 2.sine wave signal sine wave signal is greater than or equal to carrier wave signal then only signal is moved to S1 & S4. This signal is divided into two signals one signal is directly connected to S1 Another signal S4 is connected to not gate.
Similarly for another two voltages B and C all six signals are given to the voltage source converter.

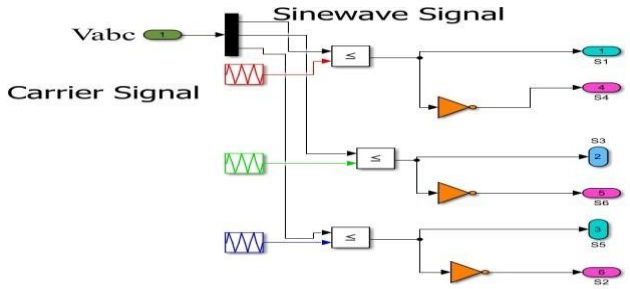


Fig 7: Simulink pulses

C. VOLTAGE SOURCE CONVERTER

It is set up as depicted in Fig. 5 and consists of two VSCs connected via a common dc terminal.

the use of two "back-to-back" VSCs with a shared DC terminal capacitor to create the UPFCOne VSC converter is coupled in series with the transmission line by an interface transformer, while the other is coupled in shunt with the line using a coupling transformer.

The fundamental purpose of the shunt-connected converter 1 is to meet the real-power requirements of converter 2, which are met by the transmission line itself. The shunt converter keeps the dc bus' voltage constant.
The capacitor, a dc energy storage component, enables the generation and absorption of actual power even while the series converter internally produces and consumes reactive power.

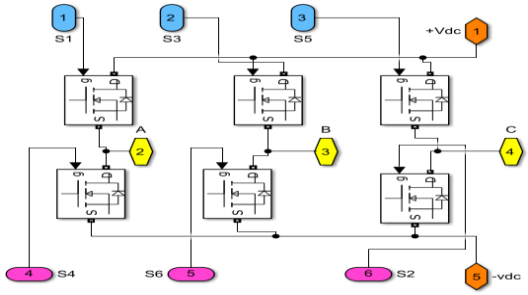


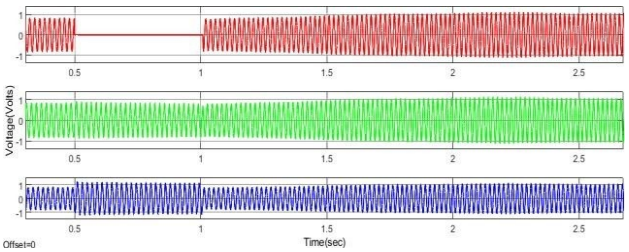
Fig 8: Simulink VSC

V. SIMULATION RESULTS

A. Case 1: LG Fault

i. Line Voltage

Without UPFC



In this, single line to ground fault is occurred in phase A at t=0.5s and cleared at t=1s. The phase A voltage is reached zero while the other two phases are unaffected. During normal conditions, the voltage is around 1pu.

With UPFC

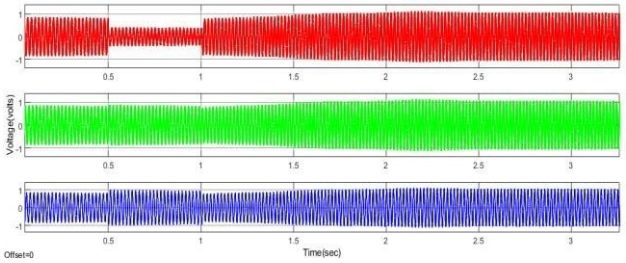
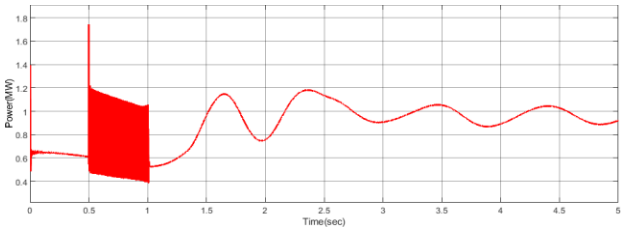


Fig 9: Line Voltage With & Without UPFC

In this, single line to ground fault is occurred in phase A at t=0.5s and cleared at t=1s. Due to the presence of UPFC, the voltage of phase A is recovered to 0.46 pu while the other two phases are unaffected. Hence 46% of system voltage is recovered due to injection of real and reactive power by upfc into the system. During normal conditions, the voltage is around 1pu.

ii. Real Power

Without UPFC



With UPFC

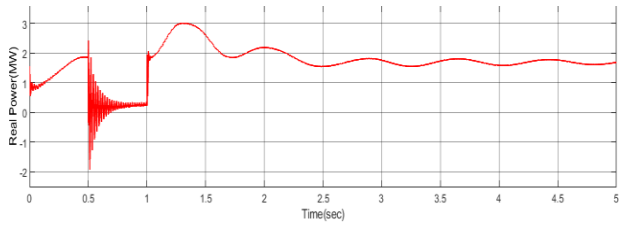


Fig 10: Real Power With & Without UPFC

The real power during the fault conditions reduces and oscillating until the fault is cleared without UPFC. Even after fault is cleared at t=1s, the power settled nearly after t=4s. With UPFC, the real power settled at t=0.7s during fault period and when fault is cleared at t=1s, the power oscillates and settled at t=2.5s.
Above the figure shows that fault is occurred at t=0.5sec, Peak overshoot 1.7pu it reduces 0.3 to 0.4sec,then fault is

cleared at t=1sec.After clearing the fault power osculation is slowly reduced. With UPFC peak overshoot is 2.5pu to -1.8pu during fault period & when fault is cleared at t=1sec, peak overshoot between 2pu to 0.1pu

iii. Load Angle

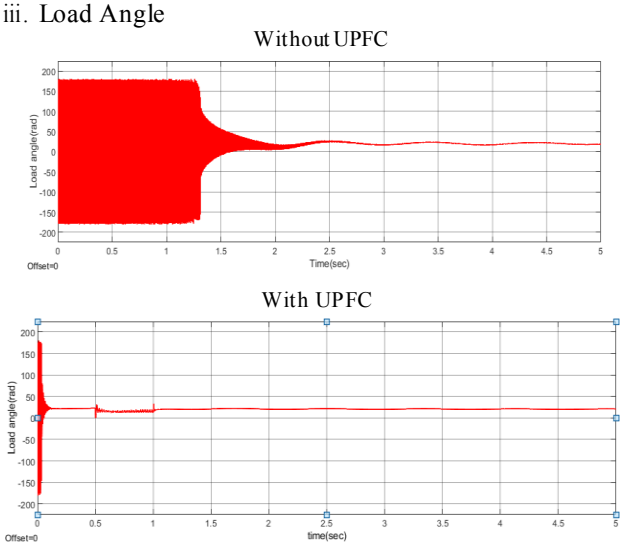


Fig 11: Load Angle With & Without UPFC

The load angle oscillates from t=0 and settled at t=2.5s without upfc whereas with upfc, it settled at t=0.05s initially and when fault occurs at t=0.5s, the oscillation settled at t=0.56s. In both cases, namely for the system without UPFC and with UPFC, the temporal response of the load angle is shown in Fig. 7.1.3. The outcomes unmistakably demonstrate how poorly damped the system is without compensation. Similarly for other two cases.

B: Case 2: LLG Fault

i. Line Voltage

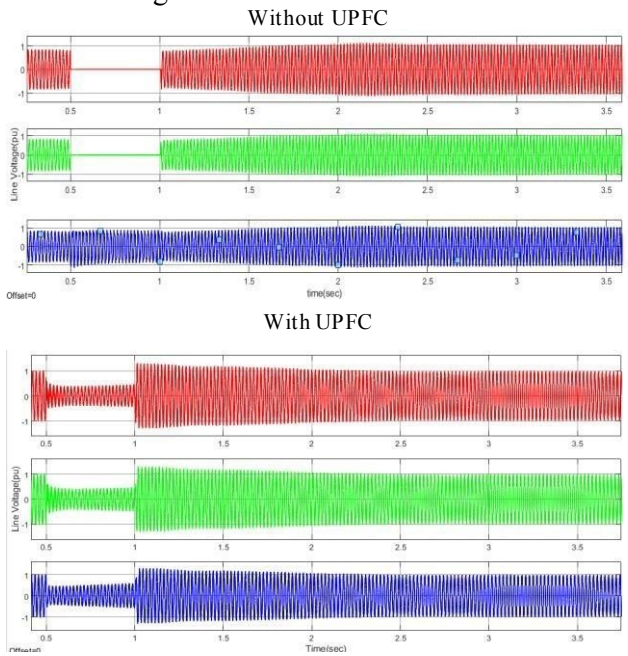


Fig 12: Line Voltage With & Without UPFC.

ii. Real Power without UPFC

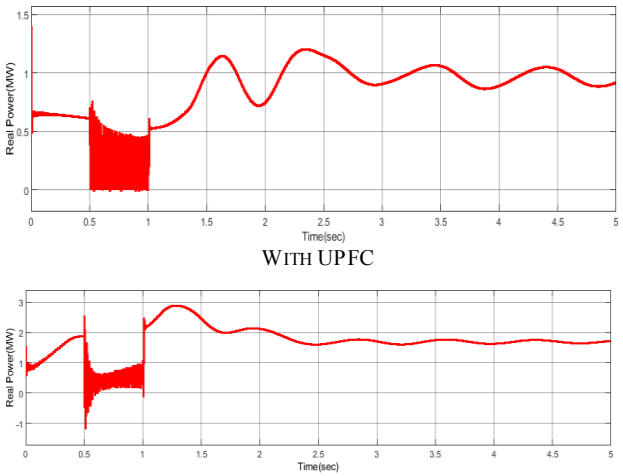


Fig 13: Real Power With & Without UPFC.

iv. Load angle

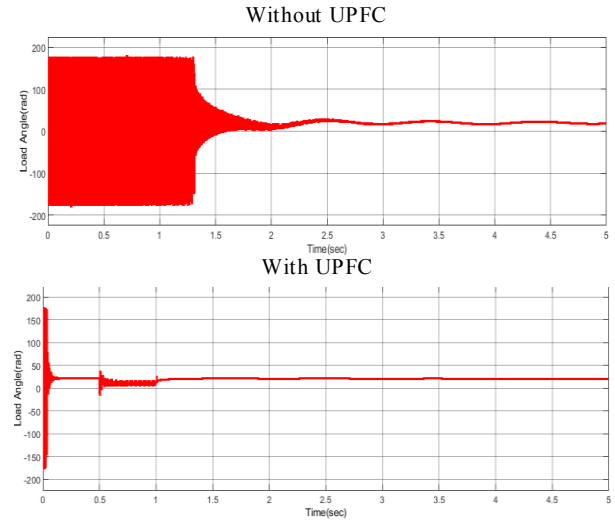


Fig 14: Load Angle With & Without UPFC.

C. Case 3: LLLG Faults

i. Line Voltage

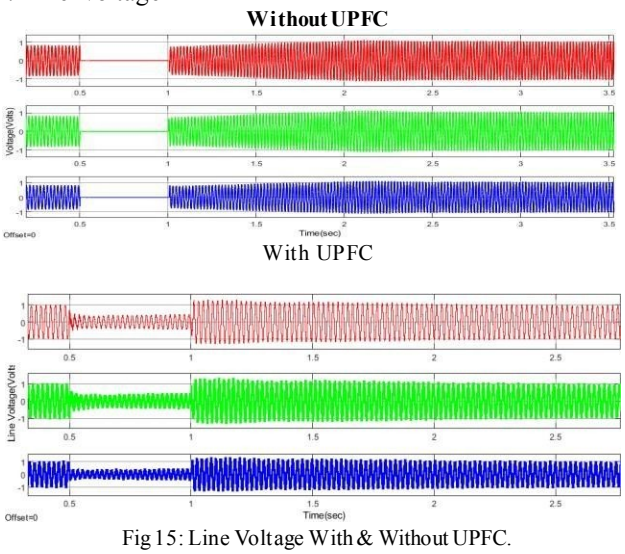
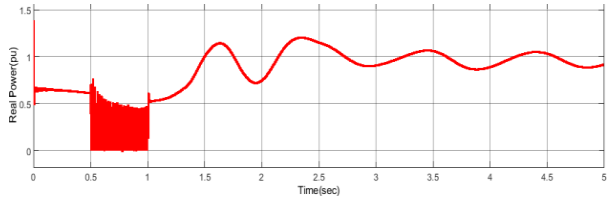


Fig 15: Line Voltage With & Without UPFC.

ii. Real Power without UPFC



With UPFC

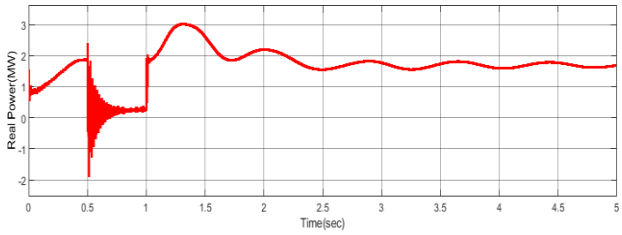
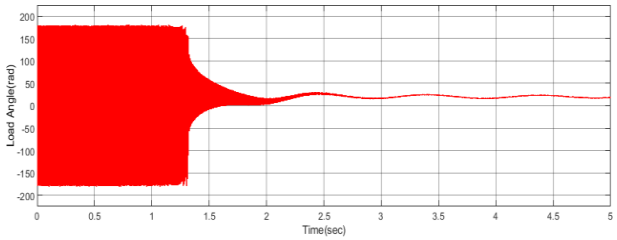


Fig 16: Real Power With & Without UPFC.

iii. Load Angle

Without UPFC



With UPFC

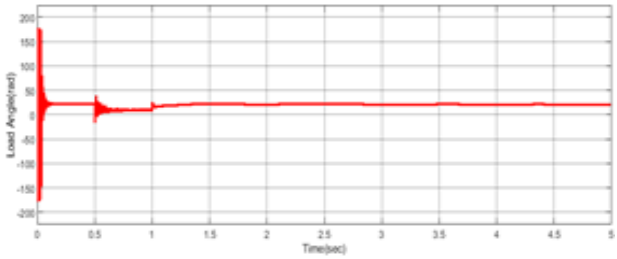


Table.1: Line Voltage

	Line Voltage(pu)		
	LG Fault	LLG Fault	LLLG Fault
Fault occurred time(sec)	0.5	0.5	0.5
Fault Cleared time(sec)	1.0	1.0	1.0
Recovered Voltage(pu)	0.46	0.43	0.4

Table.2: Real Power

	Real Power(pu)					
	LG Fault		LLG Fault		LLLG Fault	
	Without UPFC	With UPFC	Without UPFC	With UPFC	Without UPFC	With UPFC
During Fault Period Power Osculation Settled time(Sec)	0.45	0.3	0.45	0.3	0.45	0.25
After clearing Fault Period Power osculation Settled time(sec)	3.0	2.2	2.8	2.3	2.8	2.4

Table.3: Load Angle

	Real Power(pu)					
	LG Fault		LLG Fault		LLLG Fault	
	Without UPFC	With UPFC	Without UPFC	With UPFC	Without UPFC	With UPFC
During Fault Period Power Osculation Settled time(Sec)	Not settled	0.7	Not settled	0.6	Not settled	0.8
After clearing Fault Period Power osculation	2.0	1.5	2.8	1.5	2.8	1.8

CONCLUSION

The impact of a integrated power flow regulator is examined based on the decline of line voltage temporary peaks, real power transient peaks in the power, and rotor angletransient peaks, respectively, after disturbances. The proposed system with said controller is evaluated for three various types of disturbances, namely L-G,LLG, and 3-phase fault, when employed on a multi-machine system. It has been observed that a 3-phase fault affects the system more than an L-G or LL-G fault, or that a 3-phase failure is more serious than other faults. It can also notice that when a defect appears, all parameter settling times and transient peaks are shortened. Therefore, the proposed method is can be used to increase the system's stability under various failure scenarios the proposed system has given good results over state of art.

FUTURE SCOPE

- PI Controller can be replaced with fuzzy controller for better power oscillation damping.
- SSSC, STATCOM & UPFC can be replaced with UPQC for better mitigation of settling time of power oscillation.

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